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1 **Parallel genetic algorithm for optimizing run-time reconfigurable circuits**
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1 Reconfigurable computing: architectures and applications: Application-specific instruction generation for configurable processor architectures
Jason Cong, Yiping Fan, Guoling Han, Zhiru Zhang
February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**
Full text available: pdf(253.53 KB) Additional Information: full citation, abstract, references, index terms

Designing an application-specific embedded system in nanometer technologies has become more difficult than ever due to the rapid increase in design complexity and manufacturing cost. Efficiency and flexibility must be carefully balanced to meet different application requirements. The recently emerged configurable and extensible processor architectures offer a favorable tradeoff between efficiency and flexibility, and a promising way to minimize certain important metrics (e.g., execution time, co ...

Keywords: ASIP, binate covering, compilation, configurable processor, technology mapping

2 Novel ideas: Performance characterization of a hardware mechanism for dynamic optimization
Brian Fahs, Satarupa Bose, Matthew Crum, Brian Slechta, Francesco Spadini, Tony Tung, Sanjay J. Patel, Steven S. Lumetta
December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.31 MB) Additional Information: full citation, abstract, references, citings
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We evaluate the rePLay microarchitecture as a means for reducing application execution time by facilitating dynamic optimization. The framework contains a programmable optimization engine coupled with a hardware-based recovery mechanism. The optimization engine enables the dynamic optimizer to run concurrently with program execution. The recovery mechanism enables the optimizer to make speculative optimizations without requiring recovery code.We demonstrate that a rePLay configuration performing ...

3 System-level design methodology: A cosynthesis algorithm for application specific processors with heterogeneous datapaths
Yuichiro Miyaoka, Nozomu Togawa, Masao Yanagisawa, Tatsuo Ohtsuki
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**

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This paper proposes a hardware/software cosynthesis algorithm for processors with heterogeneous registers. Given a CDFG corresponding to an application program and a timing constraint, the algorithm generates a processor configuration minimizing area of the processor and an assembly code on the processor. First, the algorithm configures a datapath which can execute several DFG nodes with data dependency at one cycle. The datapath can execute the application program at the least number of cycles. ...

4 How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level

Francky Catthoor, Nikil D. Dutt, Christoforos E. Kozyrakis

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(92.68 KB) Additional Information: full citation, references, citings, index terms

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5 Performance of database workloads on shared-memory systems with out-of-order processors

Parthasarathy Ranganathan, Kourosh Gharachorloo, Sarita V. Adve, Luiz André Barroso

October 1998 **Proceedings of the eighth international conference on Architectural support for programming languages and operating systems**, Volume 33 , 32 Issue 11 , 5

Full text available: pdf(1.62 MB) Additional Information: full citation, abstract, references, citings, index terms

Database applications such as online transaction processing (OLTP) and decision support systems (DSS) constitute the largest and fastest-growing segment of the market for multiprocessor servers. However, most current system designs have been optimized to perform well on scientific and engineering workloads. Given the radically different